2nd Sem VLSI

USN | | | | | | | | | | |

12EC047

M.Tech. Degree Examination, June / July 2014
Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the concept of statistical mean in Monte Carlo simulation technique and derive the expression for number of samples 'N' required to decide the stopping criteria of simulation. **(10 Marks)**

b. Explain the need for low power VLSI design. What are the various sources of power dissipation in digital circuits? **(10 Marks)**

2 a. Obtain an expression for capacitive power, internal power and static power dissipation using Gate level analysis techniques. **(12 Marks)**

b. Discuss the effect of input signal slope and output loading capacitance on the short circuit current of an inverter. **(08 Marks)**

3 a. With neat diagrams, explain the dual bit type signal model for DSP systems. Describe a power analysis model which uses the data path module characterization to estimate the power for a single input and single output block such as a FIFO queue. **(10 Marks)**

b. Discuss the impact of transistor sizing, gate oxide thickness scaling and technology on low power electronic systems with neat diagrams. **(10 Marks)**

4 a. Derive an expression for conditional probability and frequency. **(08 Marks)**

b. Obtain the transition density and static probability of the Boolean function $y = ab + c$, given $P(a) = 0.3$, $P(b) = 0.3$, $P(c) = 0.4$, $D(a) = 1$, $D(b) = 2$ and $D(c) = 3$. **(12 Marks)**

5 a. Compare the single driver and distributed buffer scheme systems. **(10 Marks)**

b. Describe in detail, the concept of Bus invert encoding. **(10 Marks)**

6 a. What are Glitches? What is their effect on power consumption? How can they be minimized? **(08 Marks)**

b. Explain briefly the following:
i) Latches ii) Flip – Flops iii) Gate reorganization. **(12 Marks)**

7 a. Discuss zero skew and tolerable skew. How does buffer insertion and sizing help in meeting skew constraints? **(10 Marks)**

b. With neat illustrations, explain the following:
i) NORA full adder.
ii) CVSL full adder. **(10 Marks)**

8 a. Explain the principle of pre-computation architecture based on Shanon's decomposition. Also discuss signal gating. **(10 Marks)**

b. With neat illustrations, explain chip and package codesign of clock network. **(10 Marks)**

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